Appendix A
Xilinx Schematic Simulation Procedures

---

1. Double-click on the **Xilinx Foundation Project Manager** icon.

2. You will get the **Getting Started** window. Click on **Create a New Project** and then click OK. You will get the **New Project** window. Enter your project name in the box **Name**: and click on Schematic, and then choose **XC9500** (lower left device box). Click OK after this.

3. You will see a screen that shows you the directory and some default files that have been created. There are three main panes in the Project Manager window. On the upper right-hand pane, you can find a box - **Design Entry**. Click on the rightmost icon which has the shape of an AND gate (icon for the schematic editor). You now see the schematic editor in a new window. This is where you will draw your schematic.

4. The first thing you need to do is add the gates for your project. On the left side of the screen you will see an icon in the form of an AND gate - called a symbol toolbox. Click on this and the **SC Symbols** window will appear with a list of all types of components you can use. You will get a list of components in the form of a drop down menu or alternately you can go to **Mode** $\rightarrow$ **Symbols** menu item on the options bar on the top and click on symbols to get the same menu. You now have to only type the name of the component that you need. For a 2-input AND gate case, an AND gate at the bottom of the menu or scroll down through the list in the components window till you see an AND2 (2-input AND gate) and select it from the list. You then simply move the mouse and position it to wherever you require it to be placed. To position the component simply left click on the mouse. You can attach another copy of the AND gate to your cursor by simply clicking on the AND gate you just dropped. Then you can drop the new AND gate in the schematic as well. In a similar manner you can get all the components that you require for your circuit. You are now ready to connect the gates for the circuit.

5. You now need to add input and output buffers to the circuit. This is commonly referred to as adding **IBUFs** and **OBUFs** (short forms for Input Buffer and Output Buffer, respectively). These buffers indicate that the signals attached to them will actually enter and exit the FPLD chip via the I/O pins. Select IBUF for input and OBUF for output from the symbol table. Add the buffer and give it the same name as the input (or output) signal. When this is done we add **Terminals**. To do this click on the terminal button on the upper left corner of the toolbar in the **SC symbols** window in which you can type the **Terminal Name** and **Terminal Type** of each input and output, e.g. terminal name is A and type is INPUT (you can select input or output from the drop down box). Click OK and an input (or output) terminal will be attached to your cursor. Simply click on the mouse to drop the terminal into your schematic. Then add all other inputs and outputs in the same manner. The terminal names must be unique. Make sure that IBUF's and OBUF's are between the terminals and the logic gates.

6. At this point we have all the components we need so you can double-click on the upper left corner of the **SC Symbols** window to get rid of it.

7. You might at some point want to rotate the component. Go into **Mode** $\rightarrow$ **Select and Drag** menu item. Select the component you want to rotate with the mouse. Right click on the mouse and select **Symbol Properties** from the pop up menu, which appears. A new window will appear. Click on **Attributes**. You will get a menu wherein you can rotate the component by the required degrees.

Select the same and click OK.

8. The next step is to connect the gates. Select the **Mode → Draw Wires** menu item to begin the process. Say you want to connect the output of the AND gate to the input of the OR gate. Click on the output of the AND gate followed by clicking on the say upper input of the OR gate. Click on the output of the AND gate followed by clicking on the say upper input of the OR gate. A line will appear connecting the output to the input. You can continue in the manner until all the gates are connected as required by the Boolean equation.

9. Now that the schematic is done, we need to check it for errors. First, select **Options → Create Netlist**. This will check your schematic drawing and generates a machine-readable netlist, which describes what types of gates are used and how they are the connected. Next, select **Options → Integrity Test** to initiate an error check on the netlist. If the netlist has no errors, save the schematic using **File → Save As**… menu item. Now we must export the netlist. Go to the option **Options → Export Netlist** and click on it. An Export Netlist window will appear. Select Edit 200 [*.EDN] in the **Netlist Format** selection box. Click on the **Open** button. Now select **File → Exit** to close the schematic editor. On returning to the **Project Manager** we must make the filename (your file) .SCH as part of the project. Select the **Document → Add**… menu item and list items of type Schematic (*.SCH) in the dialog window. Highlight your file and click on OK. You should see your file as part of the project.

10. We are now ready for simulation. Click on the visible icon called **Simulation** at the Project Manager. This will bring up the **Logic Simulator Foundation Window** and a single, empty **Waveform Viewer** window.

11. The first thing to do is add the inputs and outputs of the circuit to the **Waveform Viewer** so that we can see what is happening as the circuit is simulated. Do this by selecting **Signal → Add Signals**… menu item. The **Component Selection for Waveform Viewer** window will appear. Click on your input name (say "A") to highlight it and then click on the **Add** button. A waveform labeled "A" will appear in the waveform viewer and a red checkmark will appear by the selected signal. We can repeat this procedure for all the inputs. Similarly do the same thing for all the outputs. Then click on the **Close** button.

12. Now the inputs and outputs are displayed, but nothing interesting is happening because all the inputs are set to logic 0. Now we need to apply a stimulus to the circuit, so naturally we select the **Signal → Add Stimulators**… menu item. This brings up the **Stimulator Selection** window. There are many number of buttons, but we are only interested in a single item: a 16-bit binary counter labeled **Bc**.

13. We now have to do a one to one mapping of all input signals to this circuit. During a simulation, the right-most 4 bits of this counter will go through every possible combination of inputs, from 0000 to 1111. Starting from the lowest input possible, we label that to the right-most bit of the counter by clicking on one of the bit circles. Do this by clicking on the name of an input in the **Waveform Viewer** window (the selected input is highlighted) and then clicking on one of the bit-circles in the **Bc** section of the **Simulator Section** window. The label of the counter bit attached to the circuit input will appear to the right of the input name in the waveform viewer. Once all the inputs are attached to the counter bits, we can click on **Close** to leave the **Simulator Selection** window. We now need to set up a parameter that controls the speed of the simulation. First, select the **Options → Preferences** menu item. Then in the **Preference** window, set the frequency of the "BO" bit of the binary counter at 50 MHz. Then click on OK. Now you can run the simulation. In case you want to run the simulation again, delete the previous waveforms using **Waveform → Delete** menu.

14. We are now ready for simulation. Set the simulation mode to **Functional** in the drop-down menu in Logic Simulator window tool-bar. This indicates we are doing a functional simulation that checks only the logical operation of our circuit and ignores detailed physical simulation timing issues. You could go for **Step by Step simulation** or **Long simulation**. Step by Step simulation is done by pressing the Step simulator waveform on the menu bar at the top of the screen. This simulates the circuit for each clock pulse. Alternatively we could go for long simulation which simulates the circuit for a fixed period of time (time period decided by you) and display the results. To do this go to **Goto options→Start Long simulation** and set the running time to 1 sec. Click on start. This will test your circuit for 1 second and the waveform will appear on the screen. Check the waveform for all the input combinations and make sure that the output is correct for all conditions. Similarly check the other circuits and show the grader the complete *one cycle of waveforms* for all the required circuits. **Caution**: When you print the waveforms, check the **Page Setup** first. You have to select "Current Page" option before you send any file to the printer. To change the size of the schematic output, check the **Print option**.

15. When you finish the experiment, save your files on your diskette and delete all your files when you leave the lab.